CLAIMS

Claims 39-76 remain in the application. No claims have been amended. Claims 1-38 have been canceled. No claims have been added.

Listing of the claims:

1-38 (Cancelled)

39. (Original) A distributed clock generator comprising:

a plurality of cells each including,

a plurality of terminals,

a cumulative clock edge detection circuit coupled to said plurality of terminals and having an output,

a delay/amplification circuit coupled to said output of said cumulative clock edge detection circuit, and

a driver circuit coupled to said plurality of terminals and to said delay/amplification circuit;

a plurality of clock wires, each of said plurality of clock wires coupling one of said plurality of terminals of one of said plurality of cells to one of said plurality of terminals of another of said plurality of cells.

40. (Original) The distributed clock generator of claim 39, wherein the plurality of cells are distributed in two dimensions.

41. (Original) The distributed clock generator of claim 39, wherein the plurality of cells are distributed in three dimensions.

42. (Original) The distributed clock generator of claim 39, wherein current travels in one direction on the plurality of clock wires.

43. (Previously Presented) The distributed clock generator of claim 39, wherein at least some of the plurality of cells and the plurality of clock wires are routed on an integrated circuit in proximity to the power supply routing on the integrated circuit.

44. (Original) The distributed clock generator of claim 39, wherein each of said plurality of cells is either a pull-up type cell or a pull-down type cell, and each of said plurality of clock wires couples one of said plurality of terminals of one of said pull-up type cells to one of said plurality of terminals of one of said pull-down type cells.

45. (Original) The distributed clock generator of claim 39, wherein each of said plurality of cells is a hybrid type cell in which each driver circuit includes at least one pull-up driver and at least one pull-down driver coupled to different ones of said plurality of terminals, and wherein said plurality of clock wires couple together the terminals coupled to pull-up drivers and pull-down drivers.

46. (Original) The distributed clock generator of claim 39, wherein each of said cumulative clock edge detection circuits phase mix clock signals received on said plurality of terminals.

47. (Original) The distributed clock generator of claim 39, wherein each of the cumulative clock edge detection circuits includes:

a plurality of transistors each having a gate, a source, and a drain, each of the gates of said plurality of transistors of said cumulative clock edge detection circuit are coupled to a different one of said plurality of terminals, the

drains of said plurality of transistors of said cumulative clock edge detection circuit are coupled to together to form a node to provide said output, and the sources of said plurality of transistors of said cumulative clock edge detection circuit are coupled some to positive and others to negative supply.

48. (Original) The distributed clock generator of claim 39, wherein each of the cumulative clock edge detection circuits includes:

a plurality of inverters each having an input and output, each of the inputs of said plurality of inverters of said cumulative clock edge detection circuit are coupled to a different one of said plurality of terminals, the outputs of said plurality of inverters of said cumulative clock edge detection circuit are coupled to together to form a node to provide said output.

49. (Original) The distributed clock generator of claim 39, wherein each of the driver circuits includes:

a plurality of transistors each having a gate, a source, and a drain, each of the drains of said plurality of transistors of said driver circuit are coupled to a different one of said plurality of terminals, the gates of said plurality of transistors of said driver circuit are shorted together, and the sources of said plurality of transistors of said driver circuit are coupled to either positive or negative supply.

50. (Original) The distributed clock generator of claim 49, wherein the sources of said plurality of transistors of some of said driver circuits are coupled to positive supply, and the sources of said plurality of transistors of others said driver circuits are coupled to negative supply.

51. (Original) The distributed clock generator of claim 49, wherein the sources of said plurality of transistors of each of said driver circuit are coupled some to positive and others to negative supply.

52. (Original) An integrated circuit comprising:

a distributed clock generator including a plurality of cells collectively having a plurality of terminal pairs, each of said plurality of terminal pairs including a charging terminal coupled to a discharging terminal to have generated there between a clock signal having its two edges defined by alternating activation/deactivation of the charging terminal and the discharging terminal, the terminals of each of said plurality of terminal pairs being part of two different ones of said plurality of cells, said plurality of cells coupled together as a result of each being coupled to certain others of said plurality of cells by said plurality of terminal pairs; and

a plurality of sets of synchronous logic each having a clock input, each clock input of each of said sets coupled to receive the clock signal of one of said plurality of terminal pairs.

53. (Previously Presented) The integrated circuit of claim 52, wherein the plurality of cells are distributed in two dimensions.

54. (Previously Presented) The integrated circuit of claim 52, wherein the plurality of cells are distributed in three dimensions.

55. (Previously Presented) The integrated circuit of claim 52, wherein current travels in one direction between each of said plurality of terminal pairs.

56. (Previously Presented) The integrated circuit of claim 52, wherein at least some of the plurality of cells and their interconnection by said plurality of terminal pairs are routed on the integrated circuit in proximity to the power supply routing on the integrated circuit.

57. (Previously Presented) The integrated circuit of claim 52, wherein each of said plurality of cells includes either multiple of the charging terminals or multiple of the discharging terminals of said plurality of terminal pairs.

58. (Previously Presented) The integrated circuit of claim 52, wherein each of said plurality of cells includes both multiple of the charging terminals and the discharging terminals of said plurality of terminal pairs.

59. (Previously Presented) The integrated circuit of claim 52, each of said plurality of cells to phase mix clock signals received on said plurality of terminals.

60. (Previously Presented) The integrated circuit of claim 59, wherein, for each of said plurality of cells, the phase mix is an average phase when the difference in the arrival times of the clock edges of said clock signals on its terminals are within a period of time roughly equivalent to the rise/fall of the clock signal.

61. (Previously Presented) The integrated circuit of claim 59, wherein, for each of said plurality of cells, the phase mix is a non-linear function of the phases of said clock signals on its terminals.

62. (Original) A cell of a distributed clock generator comprising:

a set of terminals of said cell, each of said terminals in said set being one terminal of a different terminal pair, each of said terminal pairs including a charging terminal coupled to a discharging terminal to have generated there between a clock signal having its two edges defined by alternating activation/deactivation of the charging terminal and the discharging terminal;

a cumulative clock edge detection circuit coupled to said set of terminals to determine a single clock edge transition time reflective of transitions of said clock signals on said terminals,

a driver circuit coupled to said set of terminals; and

a delay/amplification circuit, coupled to an output of said cumulative clock edge detection circuit and to said driver circuit, to cause another clock edge transition of said clock signals to substantially simultaneously occur some delay time after each of said single clock edge transition times.

63. (Original) The cell of claim 62, wherein the set of terminals of said cell are charging terminals.

64. (Original) The cell of claim 62, wherein the set of terminals of said cell are discharging terminals.

65. (Original) The cell of claim 62, wherein the set of terminals of said cell including both charging and discharging terminals.

66. (Original) The cell of claim 62, wherein said cumulative clock edge detection circuit includes:

a plurality of transistors each having a gate, a source, and a drain, each of the gates of said plurality of transistors of said cumulative clock edge detection circuit are coupled to a different one of said set of terminals, the drains of said plurality of transistors of said cumulative clock edge detection circuit are coupled to together to form a node, and the sources of said plurality of transistors of said cumulative clock edge detection circuit are coupled some to positive and others to negative supply.

67. (Original) The cell of claim 62, wherein said driver circuit includes:

a plurality of transistors each having a gate, a source, and a drain, each of the drains of said plurality of transistors of said driver circuit are coupled to a different one of said set of terminals, the gates of said plurality of transistors of said driver circuit are shorted together, and the sources of said plurality of transistors of said driver circuit are coupled to either positive or negative supply.

68. (Original) The cell of claim 67, wherein the sources of said plurality of transistors said driver circuit are coupled to positive supply.

69. (Original) The cell of claim 67, wherein the sources of said plurality of transistors of said driver circuits are coupled to negative supply.

70. (Original) The cell of claim 67, wherein the sources of said plurality of transistors of said driver circuit are coupled some to positive and others to negative supply.

71. (Original) The cell of claim 62, wherein said cumulative clock edge detection circuit to determine said single clock edges transition time based on an average phase

when the difference in the arrival times of the clock edges of said clock signals on said terminals are within a period of time roughly equivalent to the rise/fall of the clock signal.

72. (Original) The cell of claim 62, wherein said cumulative clock edge detection circuit to determine said single clock edges transition time as a non-linear function of the phases of said clock signals on said terminals.

73. (Original) The cell of claim 62, wherein said cumulative clock edge detection circuit includes smaller transistors than transistors in said driver circuit.

74. (Original) The cell of claim 62, wherein the delay time is tunable using variable delay inverters.

75. (Original) A method for generating a clock in a distributed manner, said method comprising:

each of a plurality of cells, coupled to adjacent others of said plurality of cells to receive clock signals, performing the following,

determining a moment in time based upon the arrival times of current clock edges of received clock signals;

delaying a period of time after said moment in time; and

triggering a next clock edge to said adjacent others of said plurality of cells after said delaying.

76. (Original) The method of claim 75, wherein said determining includes:

averaging the phase of said current clock edges.